Improved Test Pattern Generation for Hardware Trojan Detection using Genetic Algorithm and Boolean Satisfiability

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Outline

- Introduction
- Motivation
- Logic Testing Based Trojan Detection
- Scopes of Improvement
- Proposed New Strategy
- Experimental Results
- Conclusion

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  - May be used to amplify the effectiveness of side-channel tests [5].
- **Surprisingly, very few works has been done on Logic testing based Trojan detection**.

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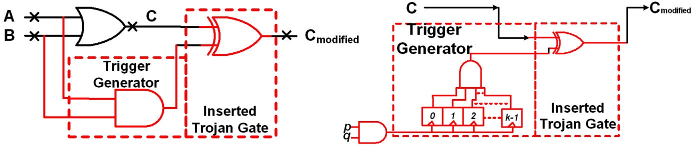
- A candidate trigger may or may not constitute a feasible trigger.

Logic Testing Based Trojan Detection: Trojan Models



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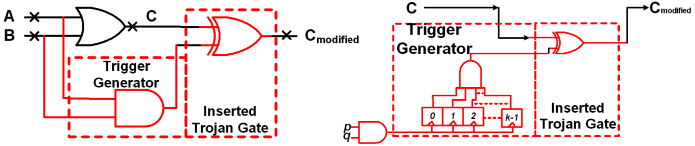

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- **Trigger inputs A and B**: internal rare nodes inside the circuit.
- **Sequential Trojan**: activated if rare logic condition occurs *k* times.

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- Chakraborty et.al presented an automatic test pattern generation (ATPG) scheme called *MERO* (*CHES* 2009) [5].

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- ***N-detect*** ATPG scheme was proposed:
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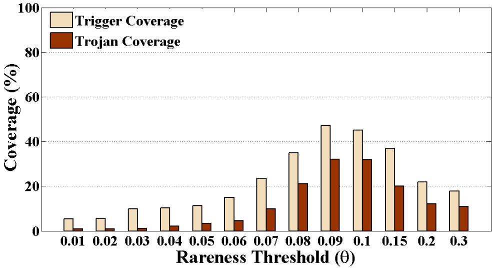
- **Assumption**: Multiple individual activation also increases the probability of simultaneous activation.

Scopes of Improvement



- **Trojan test set**: only “hard-to-trigger” Trojans with triggering probability (P_{tr}) below 10^{-6}.

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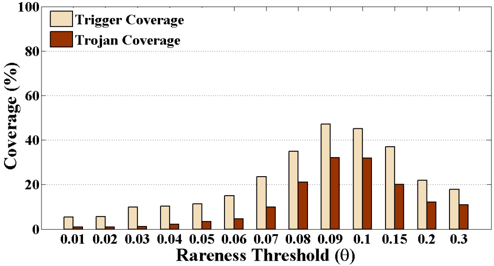

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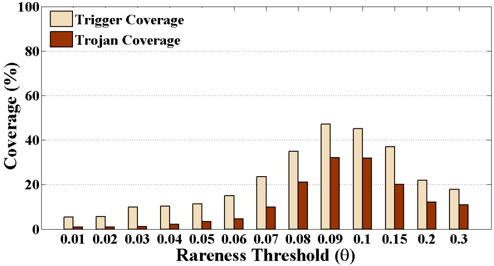

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- Test Coverage of *MERO* is consistently below 50% for circuit c7552.

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- Refinement of the test set considering the “payload effect” of Trojans: **a fault simulation based approach**.

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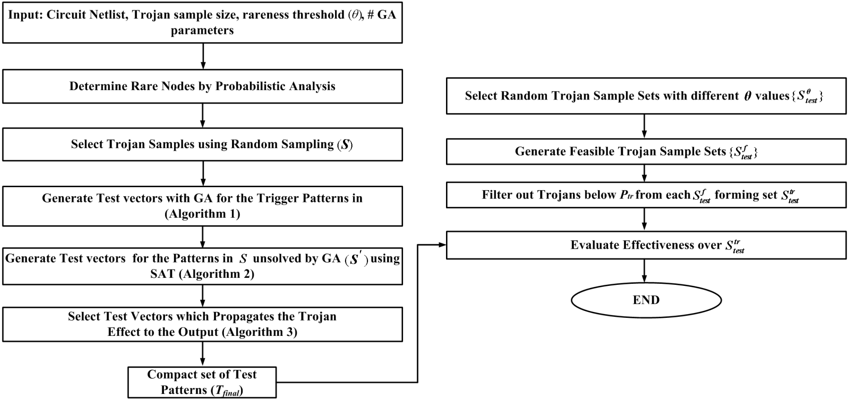
- We combine the “best of both worlds” for GA and SAT.

Proposed Scheme



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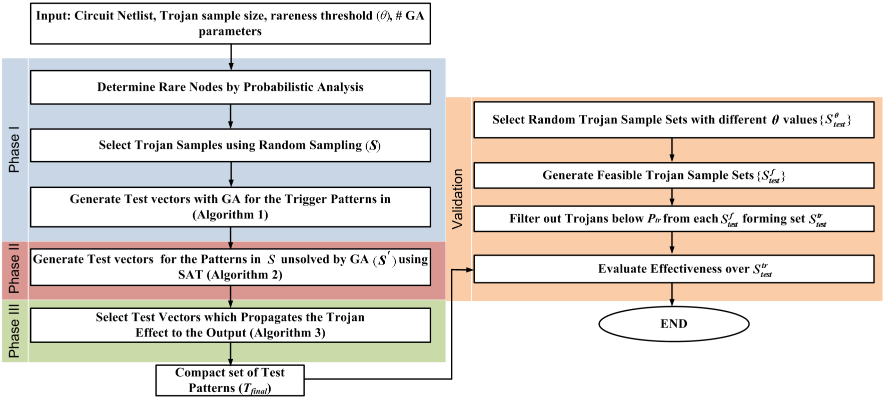

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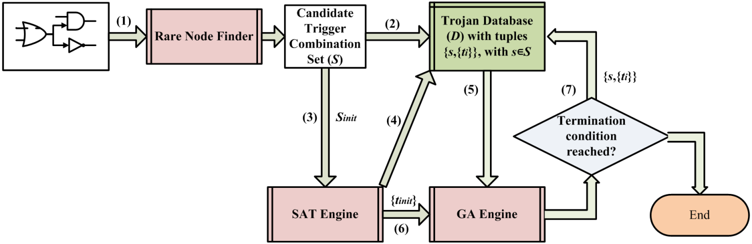

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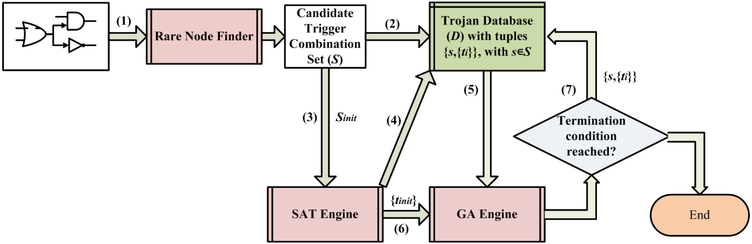

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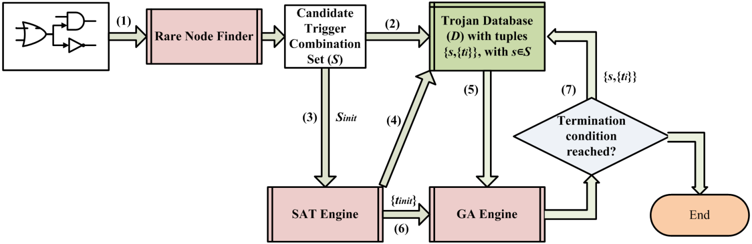

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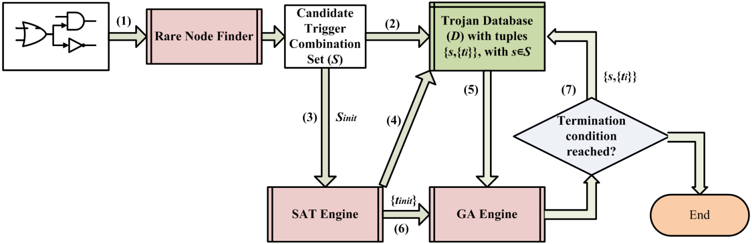

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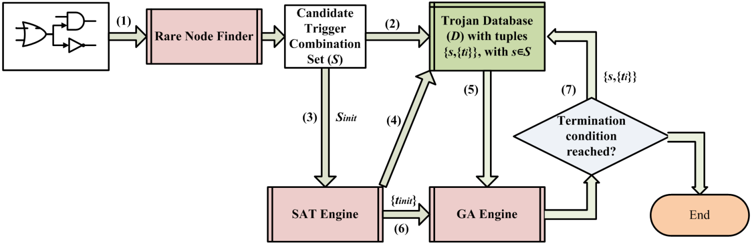

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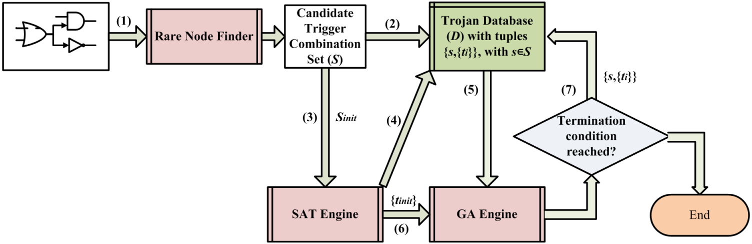

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- **Termination**: if either 1000 generations has been reached or a specified $\#T$ number of test vectors has been generated.

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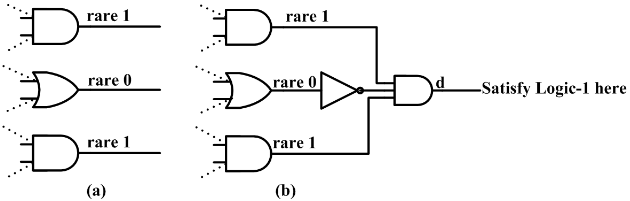

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Goal 2

- An effort to generate test vectors for hard-to-trigger combinations.

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Fitness Function

$$f(t) = R_{count}(t) + w * I(t) \quad (1)$$

- $f(t)$: fitness value of a test vector t.
- $R_{count}(t)$: the number of rare nodes triggered by the test vector t.
- w : constant scaling factor (> 1).
- $I(t)$: *relative improvement* of the database $\mathcal{D}$ due to the test vector t.

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Relative Improvement

$$I(t) = \frac{n_2(s) - n_1(s)}{n_2(s)} \tag{2}$$

- $n_1(s)$: number of test patterns in bin s before update
- $n_2(s)$: number of test patterns in bin s after update.

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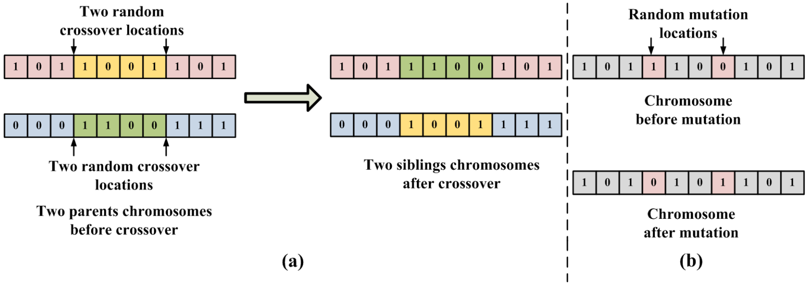

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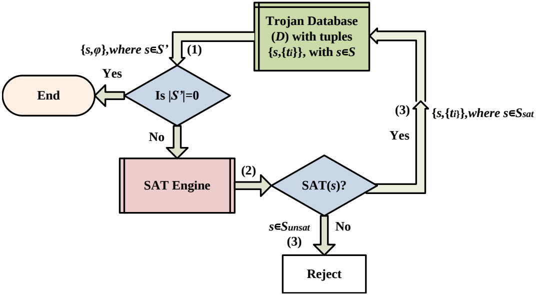

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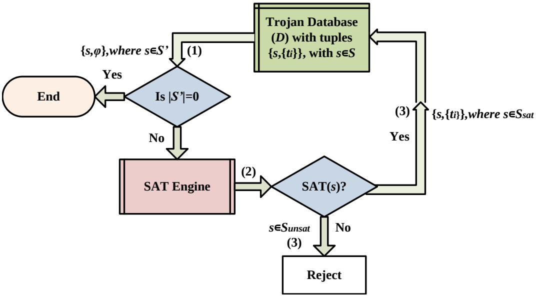

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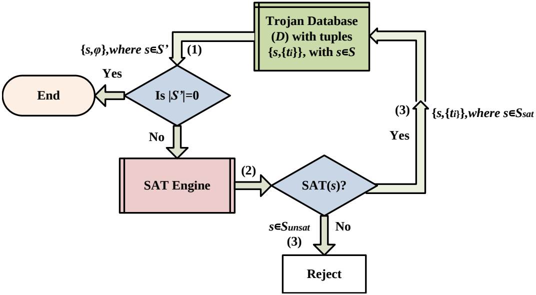

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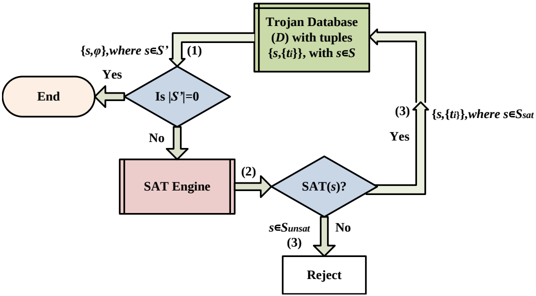

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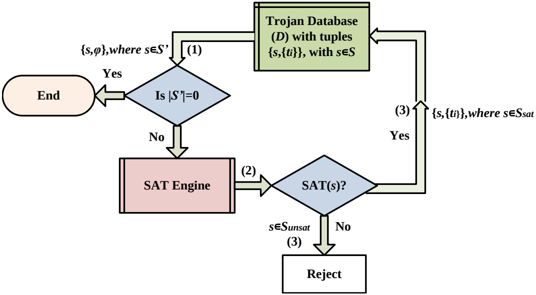

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- In general, a successful Trojan triggering event provides no guarantee regarding its propagation to the primary output to cause functional failure of the circuit.

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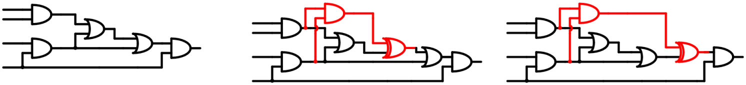

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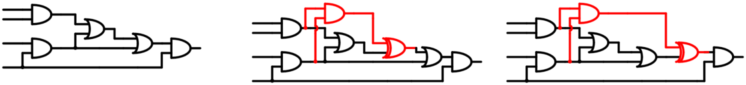

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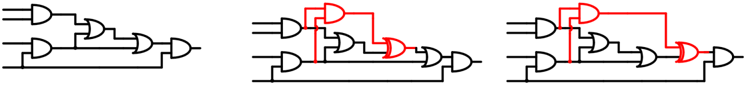

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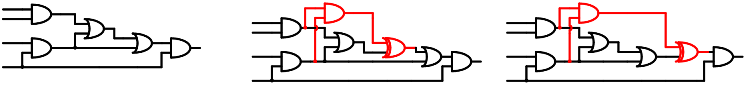

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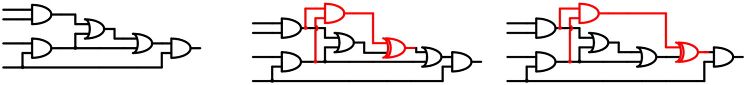

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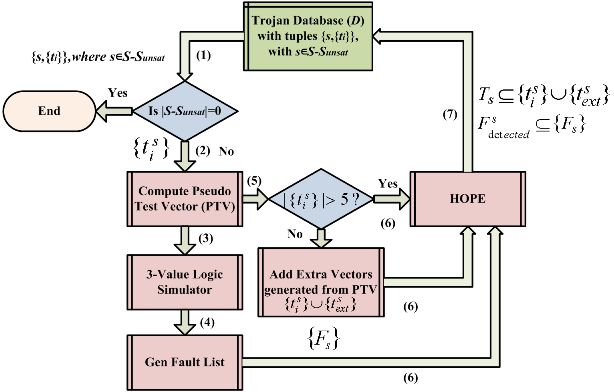

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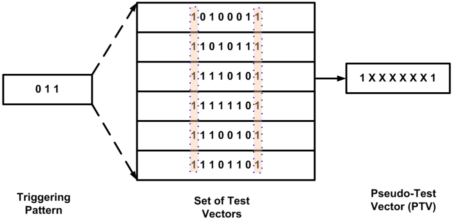

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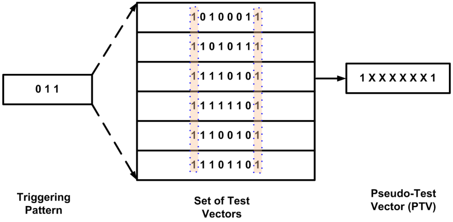

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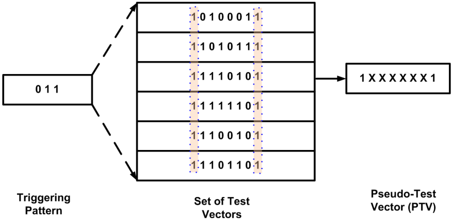

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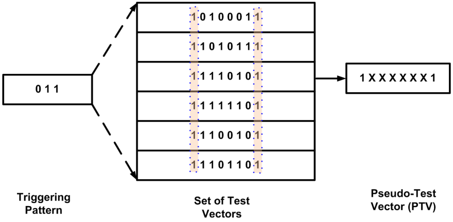

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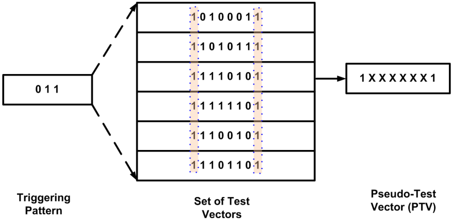

- For each set of test vectors ($\{t_i^s\}$) corresponding to a triggering combination (s), we find out the primary input positions which remains static (logic-0 or logic-1).
- Rest of the input positions are marked as "don't care" (X).
- A 3-value logic simulation is performed with this PTV and values of all internal nodes are noted down (0,1, or X).

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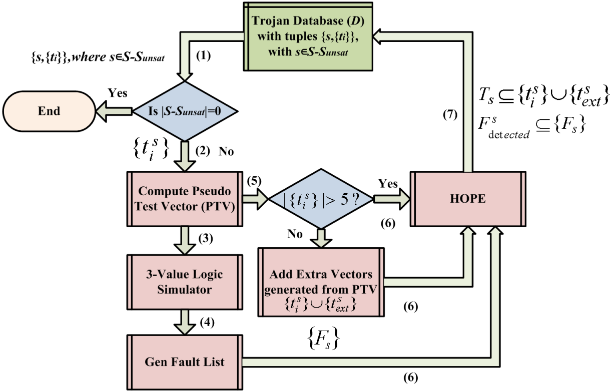
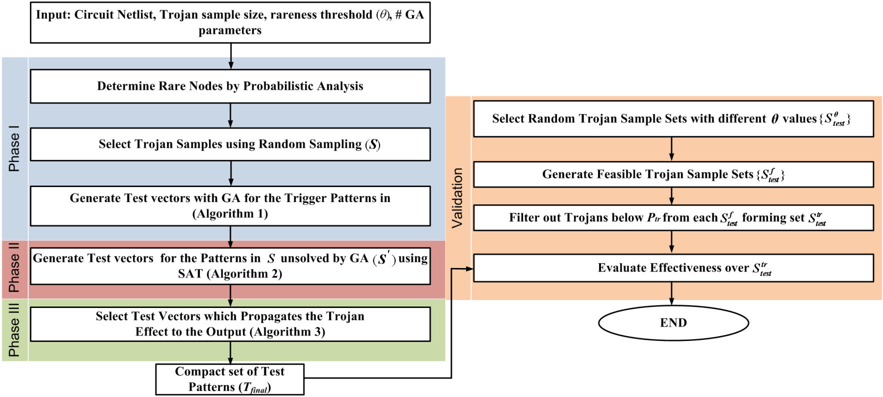


Experimental Results: Setup



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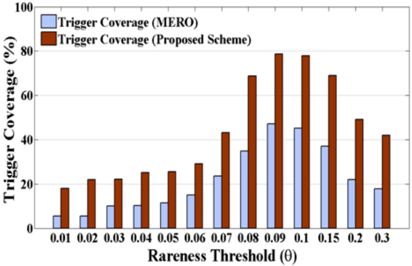
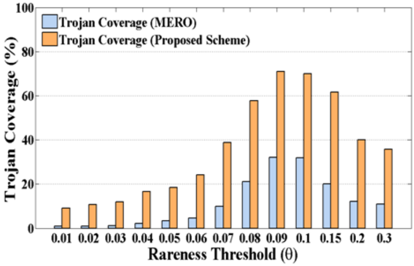
Experimental Results: circuit c7552



(a) Trigger Coverage



(b) Trojan Coverage

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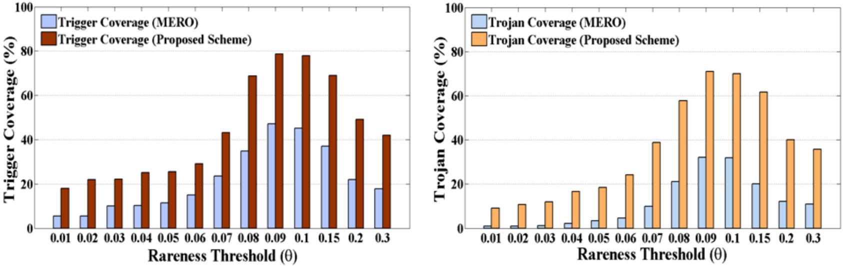

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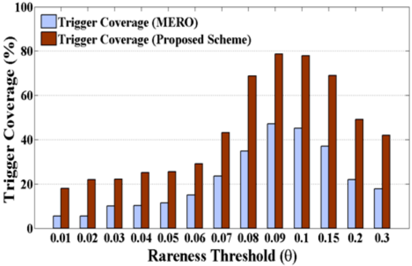

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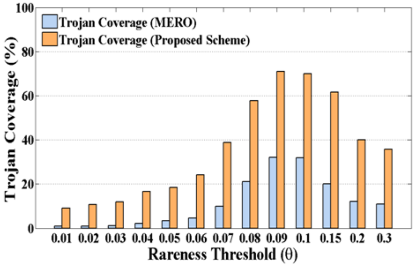

(b) Trojan Coverage

- Proposed scheme outperforms *MERO* to a significant extent.

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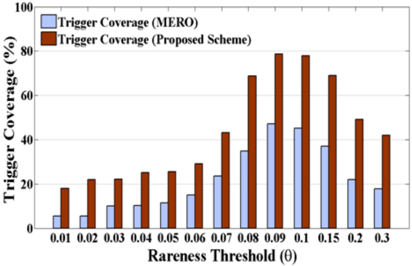

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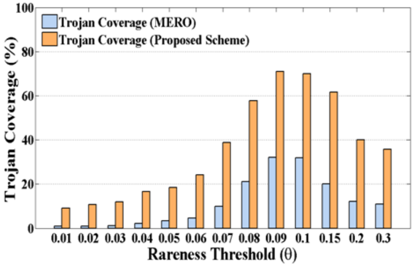

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- Proposed scheme outperforms *MERO* to a significant extent.
- The coverage trend is similar to *MERO* and the best operating point is 0.1.

Experimental Results on ISCAS Benchmarks

Table: Comparison of the proposed scheme with *MERO* with respect to testset length.

Ckt.	Gates	Testset (before Algo.-3)	Testset (after Algo.-3)	Testset (*MERO*)	Runtime (sec.)
c880	451	6674	5340	6284	9798.84
c2670	776	10,420	8895	9340	11299.74
c3540	1134	17,284	16,278	15,900	15720.19
c5315	1743	17,022	14,536	15,850	15877.53
c7552	2126	17,400	15,989	16,358	16203.02
s15850	9772	37,384	37,052	36,992	17822.67
s35932	16065	7849	7078	7343	14273.09
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- Terminating condition of GA was set by the number of test vectors which *MERO* generates in is standard setup ($N = 1000$).
- Sequential circuits were considered in full-scan mode.

Experimental Results on ISCAS Benchmarks

Table: Comparison of trigger and Trojan Coverage among *MERO* patterns and patterns generated with the proposed scheme with $\theta = 0.1$; $N = 1000$ (for *MERO*) and for trigger combinations containing up to four rare nodes.

Ckt.	*MERO*		Proposed Scheme	
	Trigger Coverage	Trojan Coverage	Trigger Coverage	Trojan Coverage
c880	75.92	69.96	96.19	85.70
c2670	62.66	49.51	87.15	75.82
c3540	55.02	23.95	81.55	60.00
c5315	43.50	39.01	85.91	71.13
c7552	45.07	31.90	77.94	69.88
s15850	36.00	18.91	68.18	57.30
s35932	62.49	34.65	81.79	73.52
s38417	21.07	14.41	56.95	38.10

Experimental Results on ISCAS Benchmarks

Table: Coverage comparison between *MERO* and the proposed Scheme for sequential Trojans.

Ckt.	Trig. Cov. for Proposed Scheme		Trig. Cov. for *MERO*	
	Trojan State Count		Trojan State Count	
	2	4	2	4
s15850	64.91	45.55	31.70	26.00
s35932	78.97	70.38	58.84	49.59
s38417	48.00	42.17	16.11	8.01

Ckt.	Troj. Cov. for Proposed Scheme		Troj. Cov. for *MERO*	
	Trojan State Count		Trojan State Count	
	2	4	2	4
s15850	46.01	32.59	13.59	8.95
s35932	65.22	59.29	25.07	15.11
s38417	30.52	19.92	9.06	2.58

Conclusion

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- ATPG for Hardware Trojan detection is an important and less explored direction of research.
- State-of-the-art techniques were not good enough.
- Proposed scheme significantly improves the performance of the ATPG mechanism.
- The generated Trojan database can be further used for Trojan diagnosis.
- Test vectors generated by the proposed scheme may also be utilized to improve the efficiency of side channel analysis based Trojan detection schemes.

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Questions?

Thank You...

Backup Slides

Experimental Results on ISCAS Benchmarks

Table: Trigger and Trojan coverage at various stages of the proposed scheme. at $\theta = 0.1$ for random sample of Trojans upto 4 rare node triggers (Sample size is $100,000$ for combinational circuits and $10,000$ for sequential circuits).

Ckt.	GA only		GA + SAT		GA + SAT + Algo. 3	
	Trig. Cov.	Troj. Cov.	Trig. Cov.	Troj. Cov.	Trig. Cov.	Troj. Cov.
c880	92.12	83.59	96.19	85.70	96.19	85.70
c2670	81.63	69.27	87.31	75.17	87.15	75.82
c3540	80.58	57.21	82.79	59.07	81.55	60.00
c5315	83.79	64.45	85.11	65.04	85.91	71.13
c7552	73.73	64.05	78.16	68.95	77.94	69.88
s15850	64.91	51.95	70.36	57.30	68.18	57.30
s35932	81.15	71.77	81.90	73.52	81.79	73.52
s38417	55.03	29.33	61.76	36.50	56.95	38.10

Probabilistic Analysis to find out Rare Nodes