

RUHR-UNIVERSITÄT BOCHUM

Horst Görtz Institute for IT-Security

# Assessment of Hiding the Higher-Order

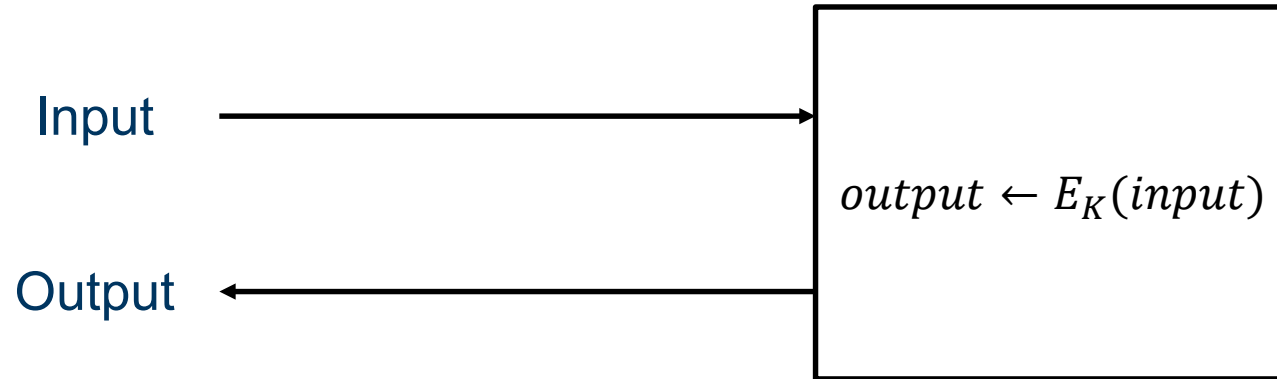
--what are the achievements versus overheads?--

Amir Moradi, Alexander Wild

September 16, 2015

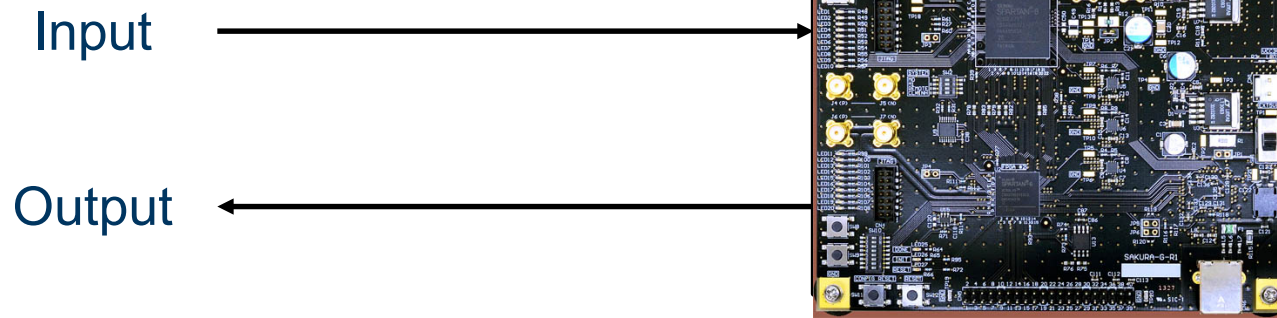
# Intro to SCA

## ATTACK MODEL



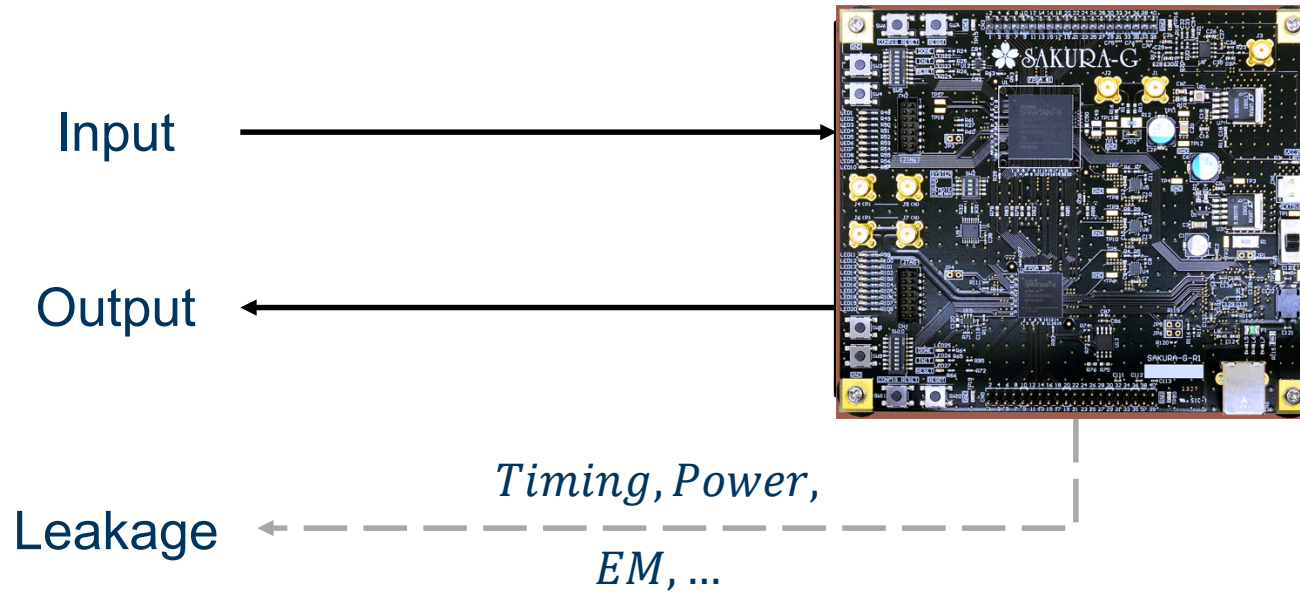
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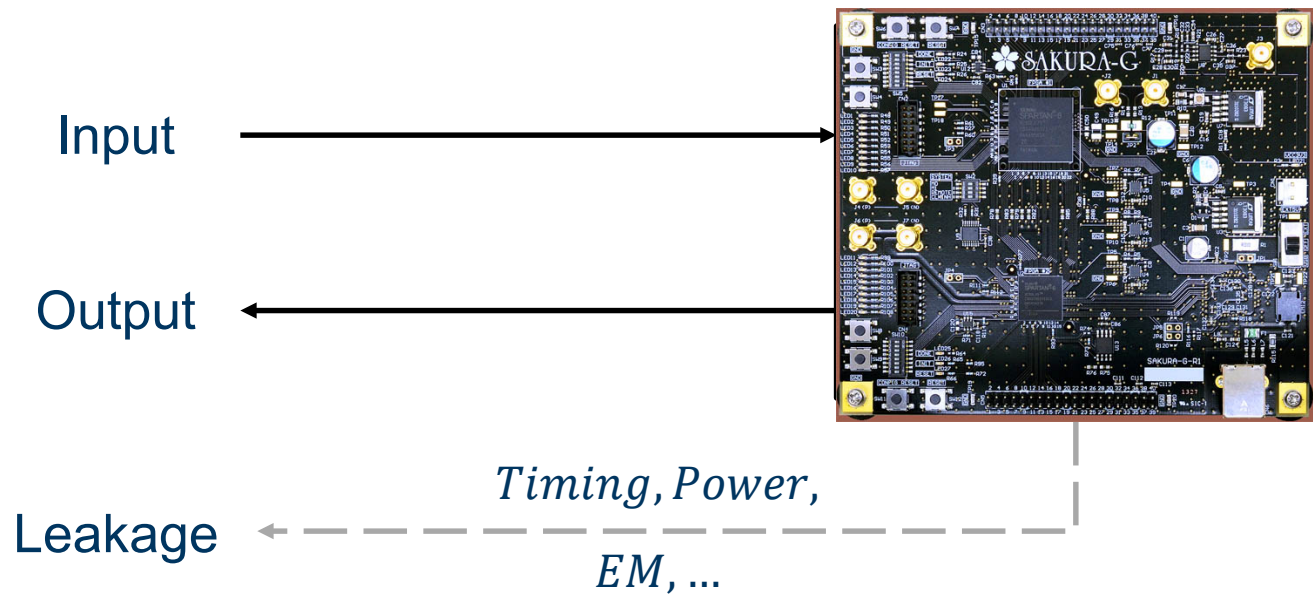
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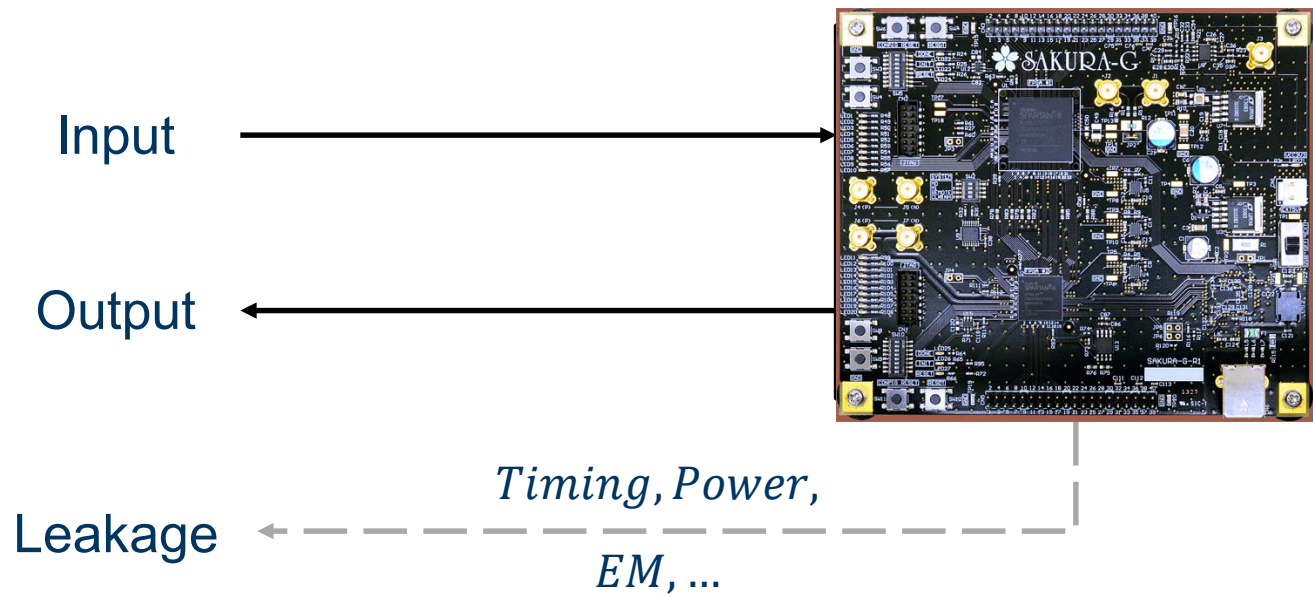
## COUNTERMEASURES

### Masking



# Intro to SCA

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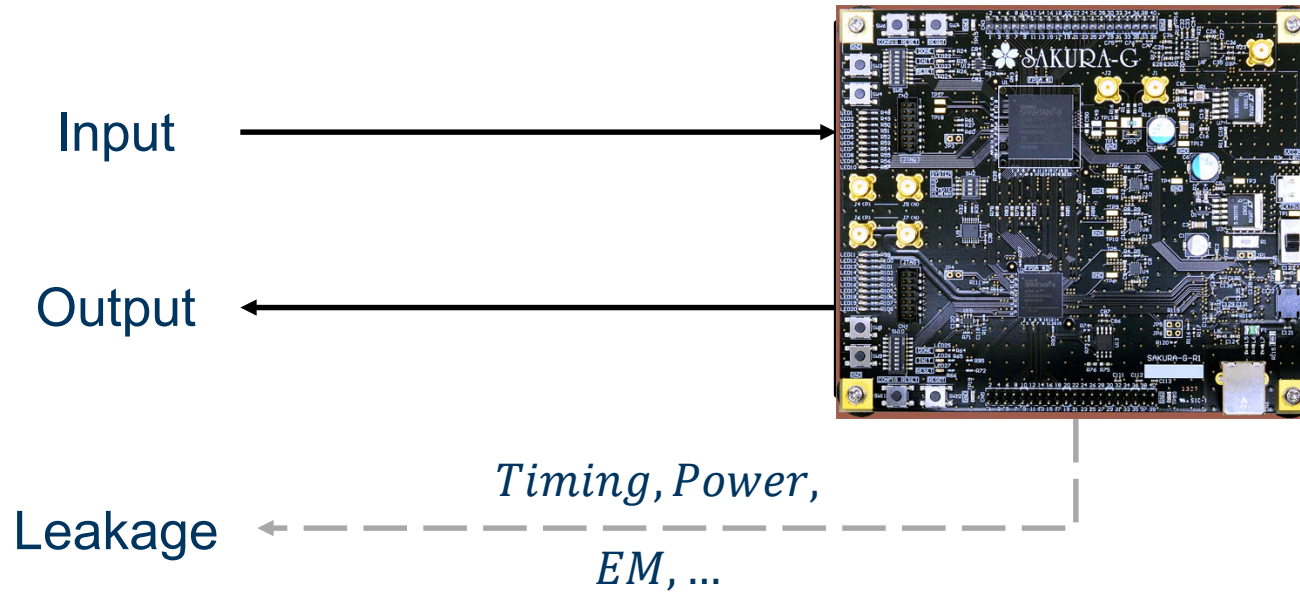


### Hiding



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## ATTACK MODEL



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### Hiding



### Rekeying



# Introduction

## MOTIVATION



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### ■ Threshold Implementation provide 1<sup>st</sup>-order security.

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- Expected hardening on each statistical order.
- Higher-Order attacks are hard on noisy traces. Power-Equalization schemes reduce signal level and have the same effect.

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### ■ Combine hiding with TI

- Often suggested but “never” examined.

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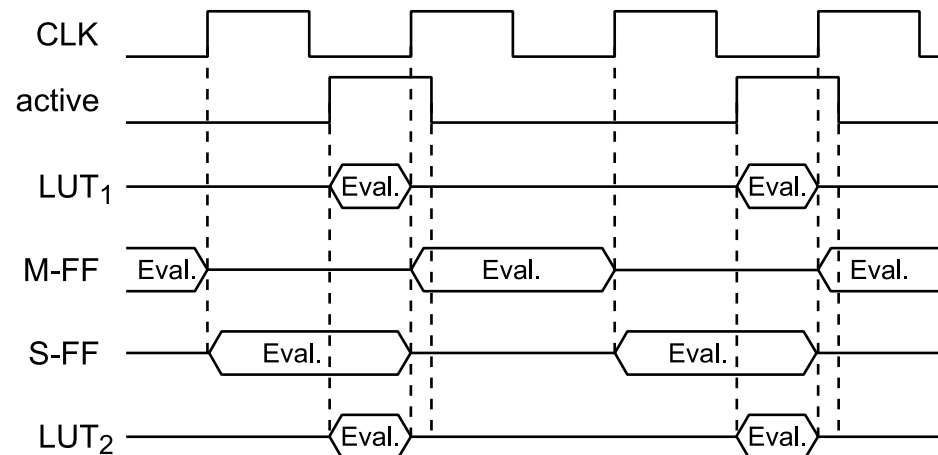
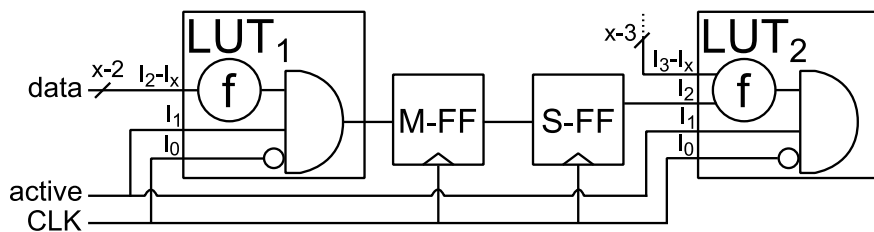
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A. Wild, A. Moradi, and T. Güneysu. GliFreD: Glitch-Free Duplication – Towards Power-Equalized Circuits on FPGAs. Cryptology ePrint Archive, Report 2015/124.

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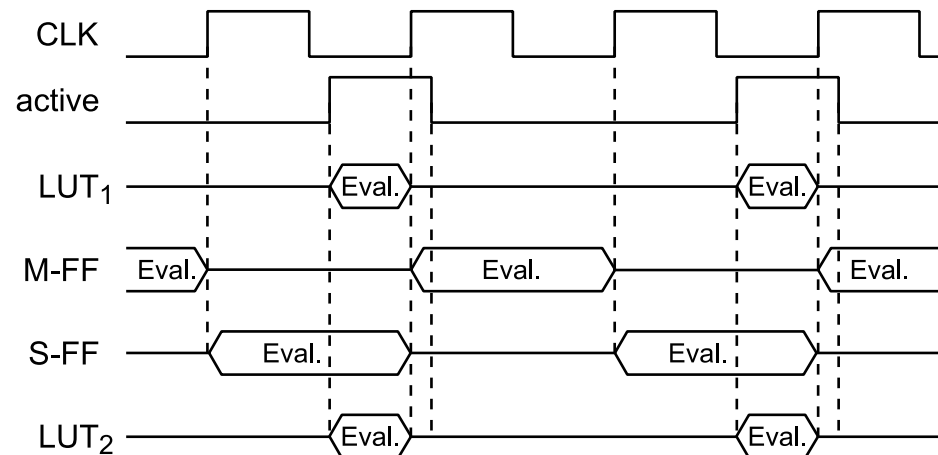
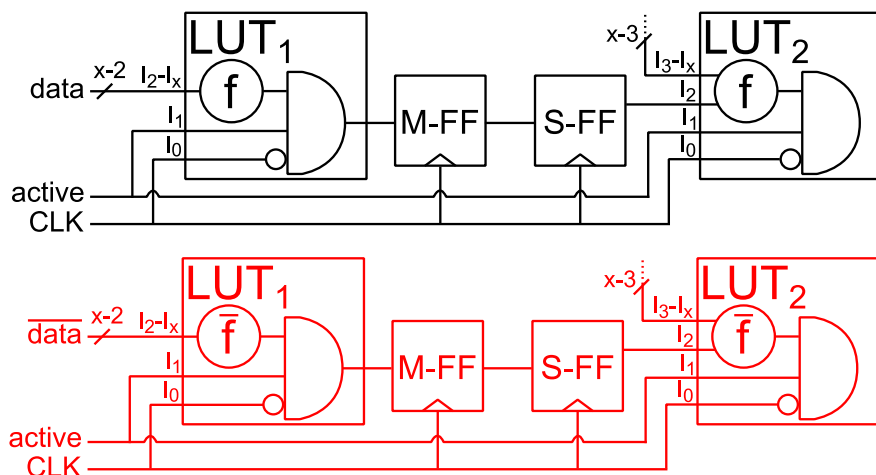
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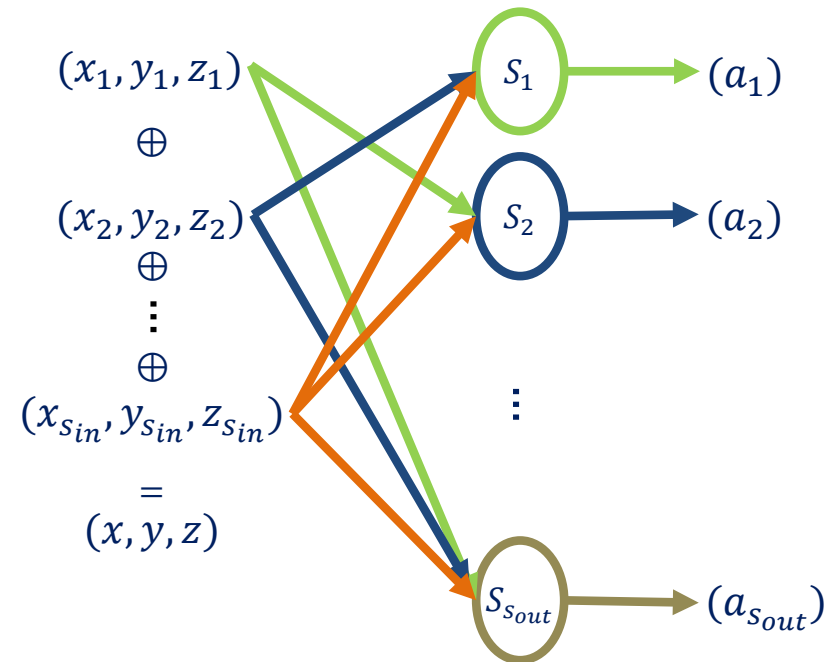
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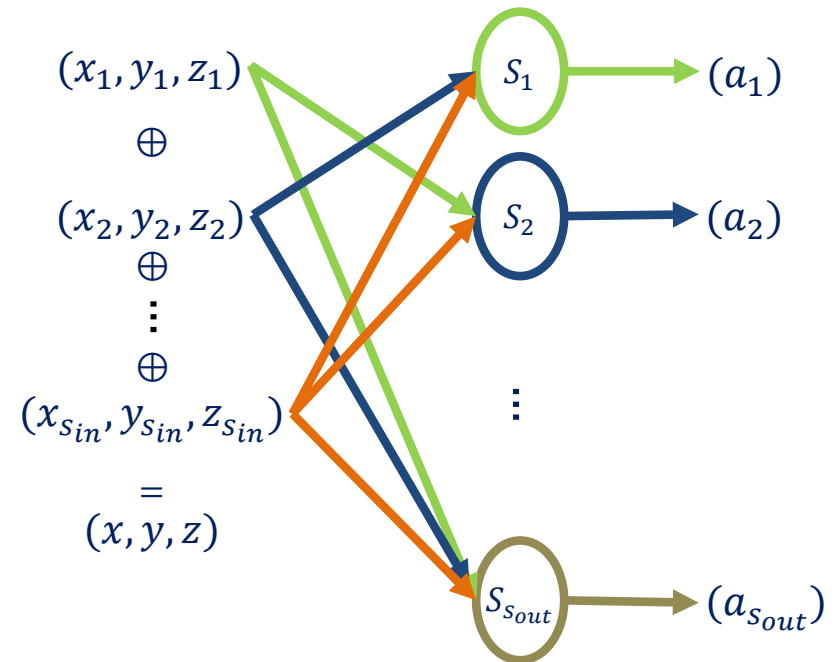


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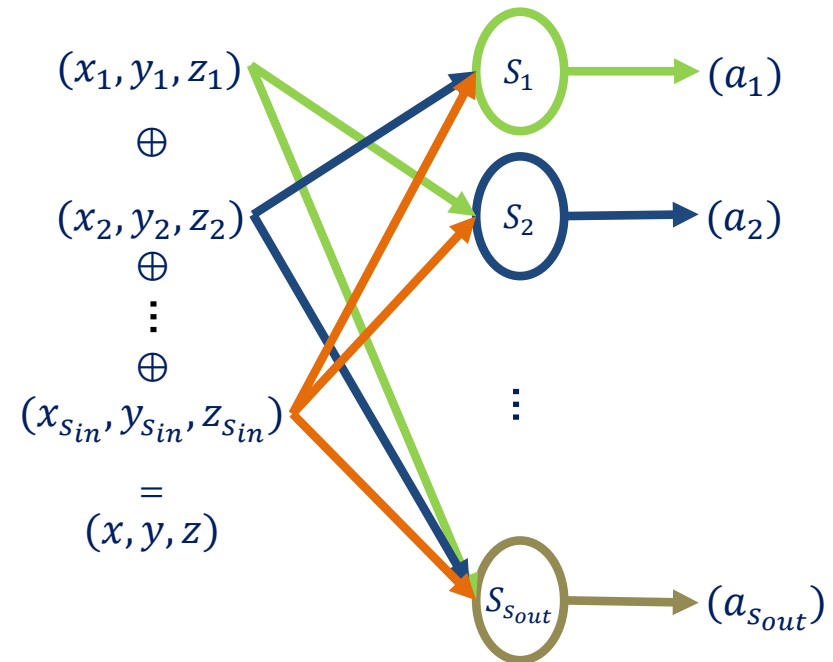


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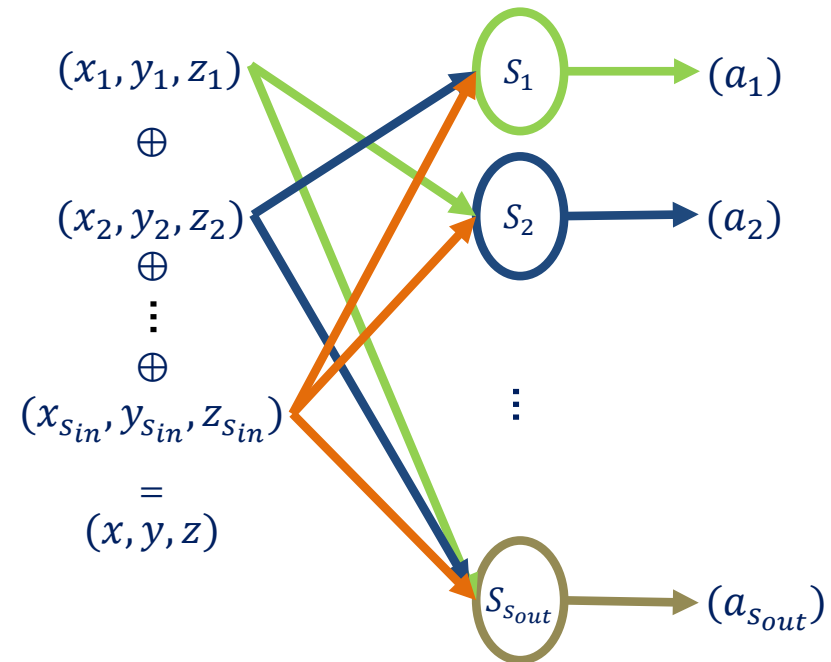


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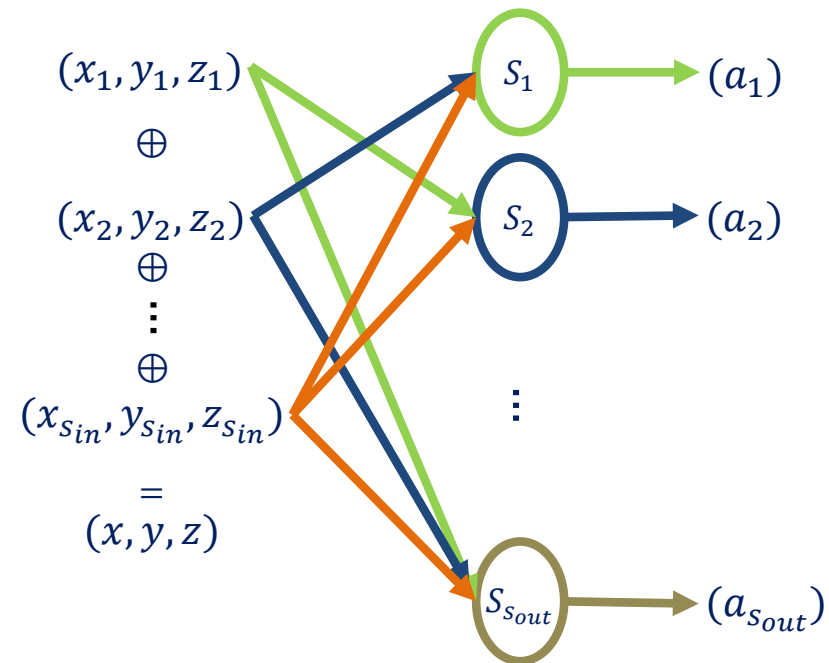


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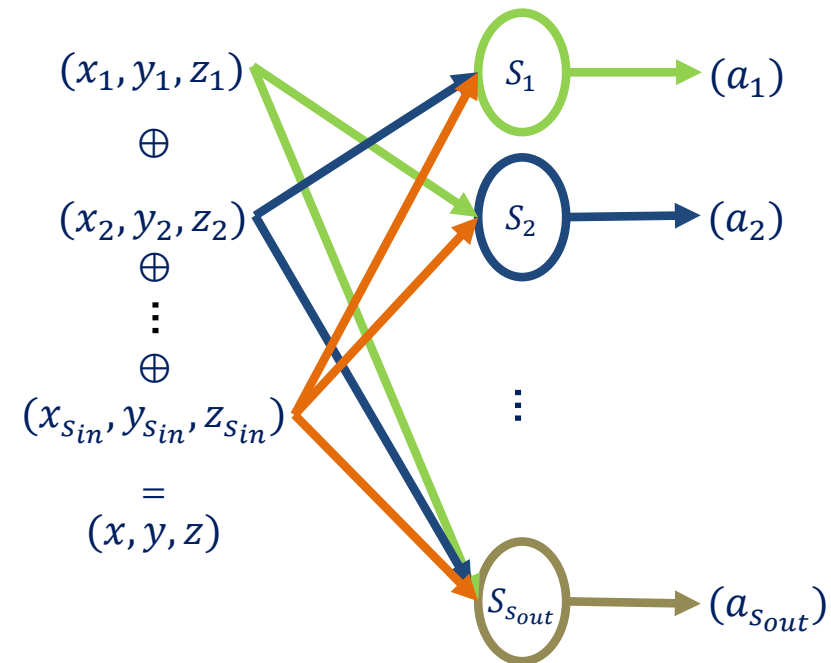


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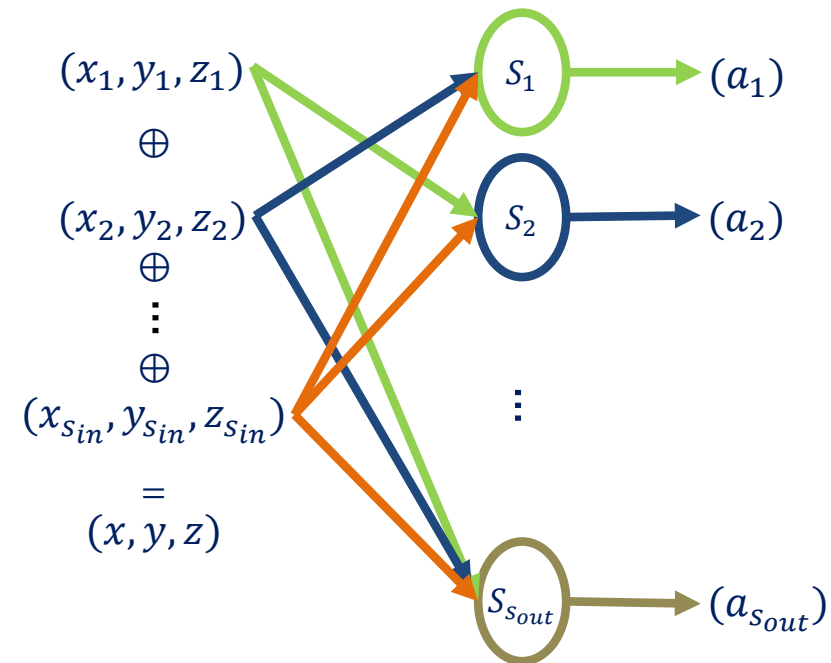


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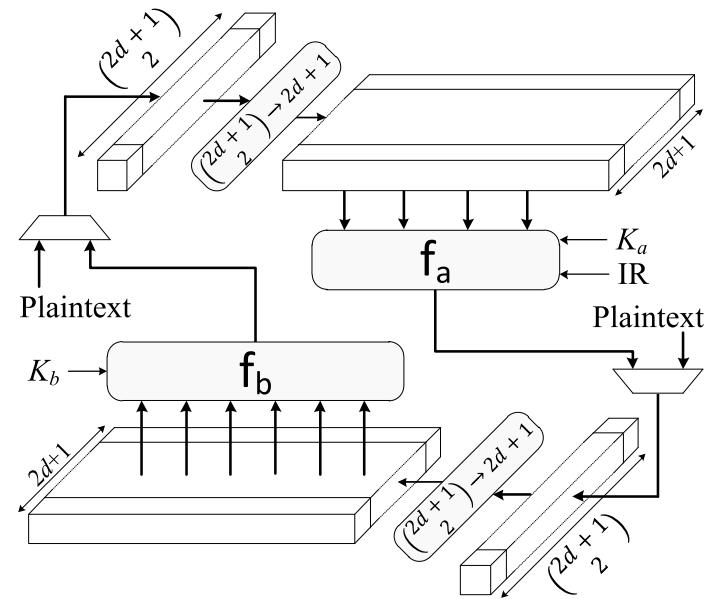




# Case Studies

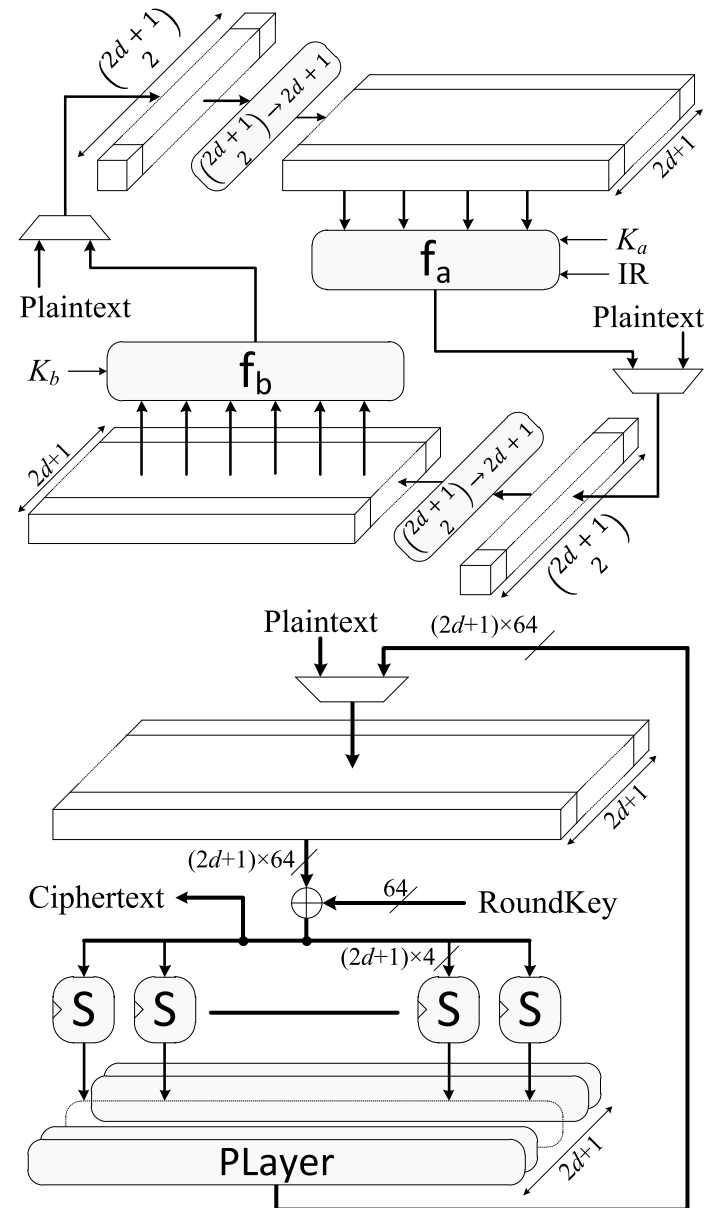
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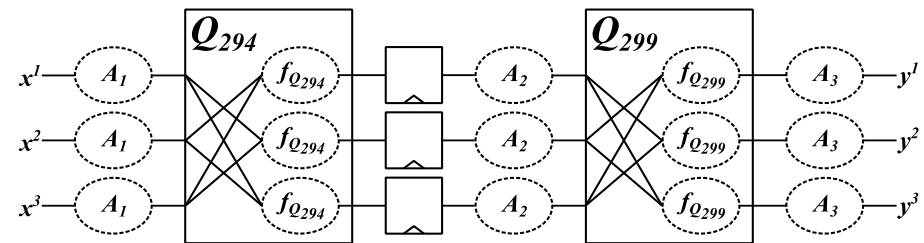
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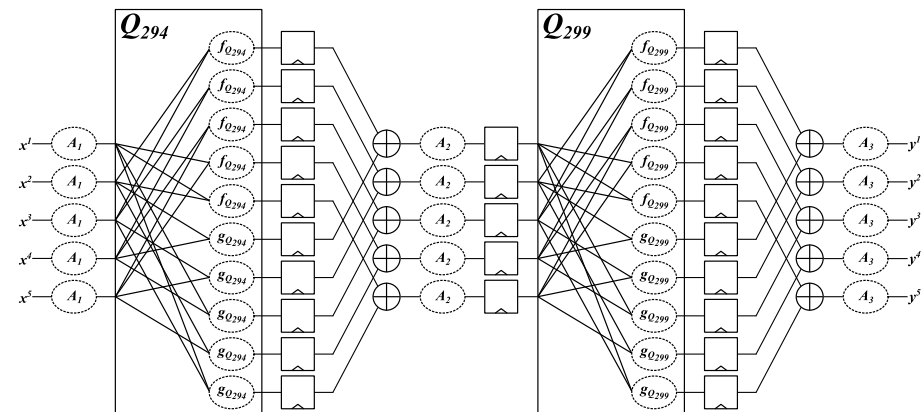
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KATAN-1 <sup>st</sup>	34	96	225.38	273	1	26.42
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KATAN-1 <sup>st</sup> -G	114	548	438.21	546	1	25.68
PRESENT-1 <sup>st</sup>	808	384	206.61	64	2	413.22
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Xilinx Spartan-6 FPGA of SAKURA-G

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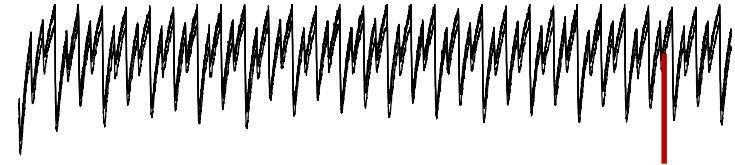
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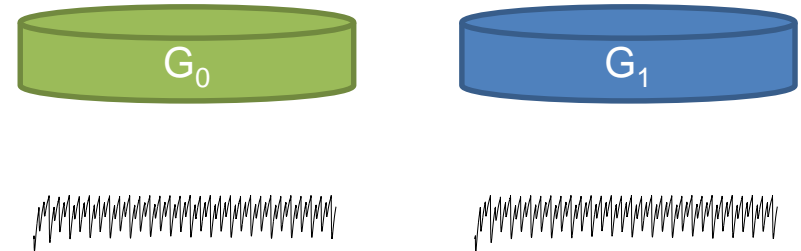
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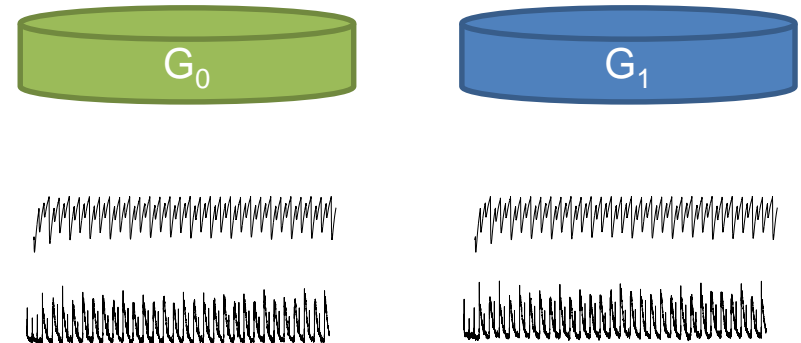
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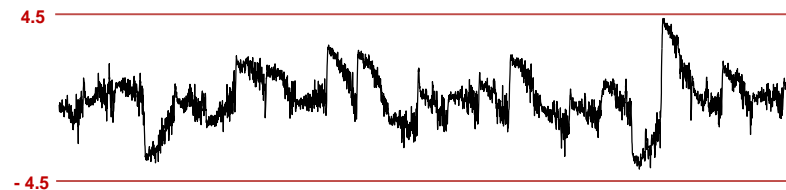


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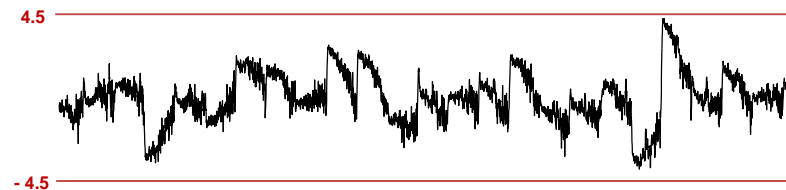
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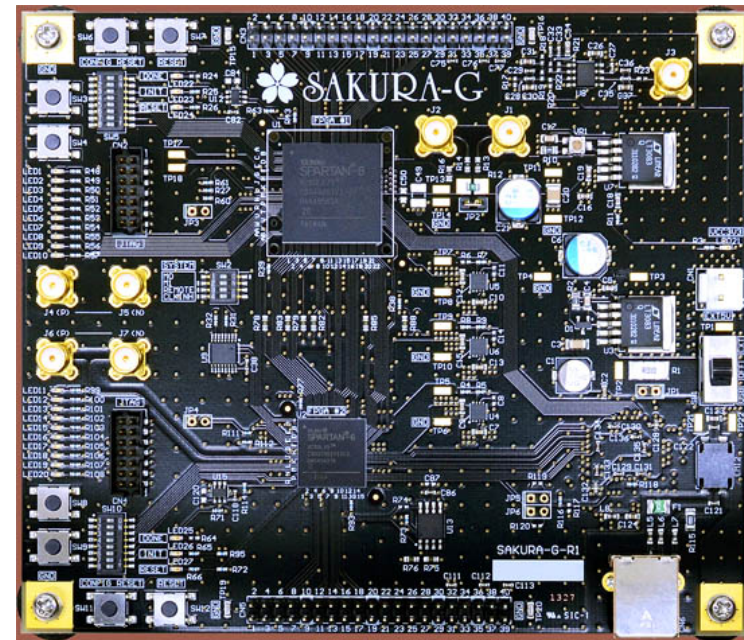
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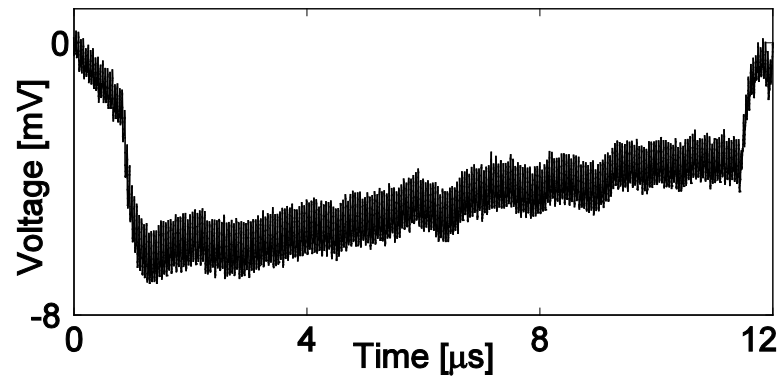
## SETUP

- SAKURA-G
- Running the designs @ 24MHz
- Measurements with 500MS/s
- Several million traces
- Non-specific  $t$ -test
  - 1<sup>st</sup>- to 5<sup>th</sup>-order
  - Depends on used shares

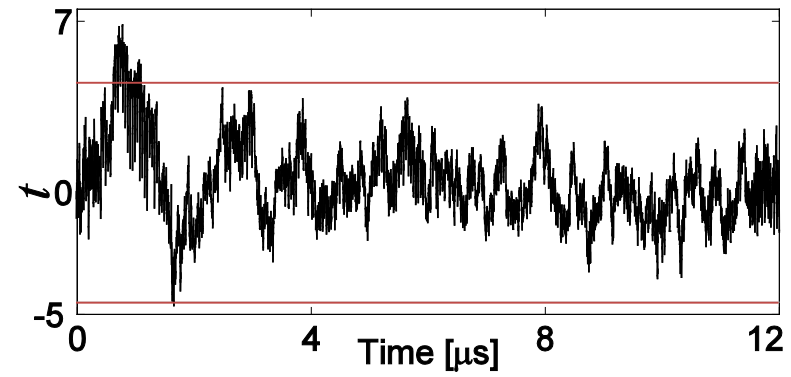


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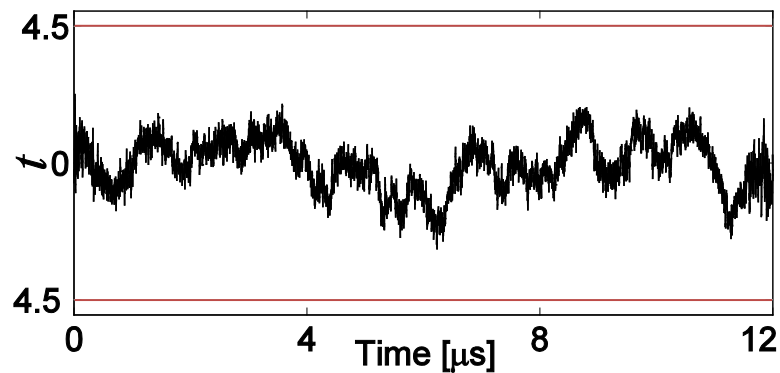
## KATAN-1<sup>ST</sup> (1 MILLION TRACES)



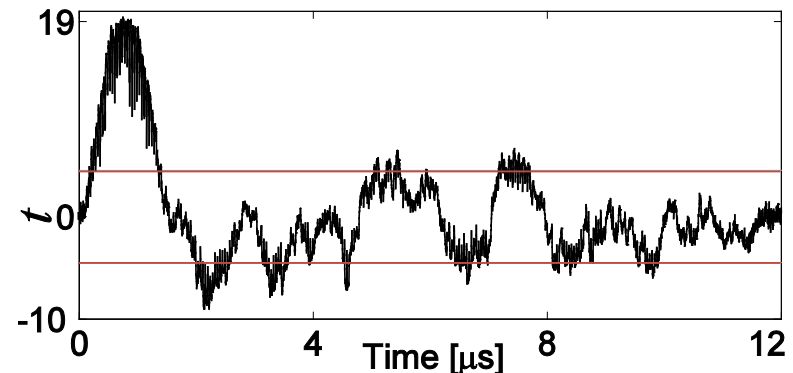
Sample Trace



Second-Order



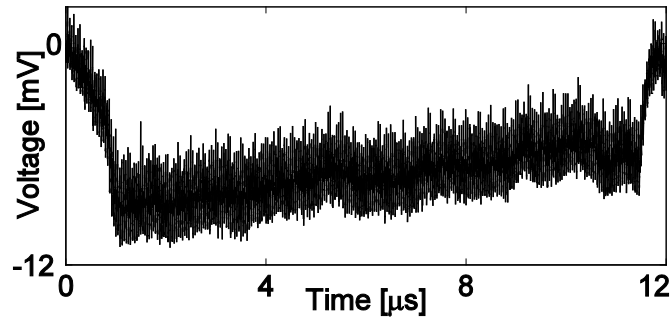
First-Order



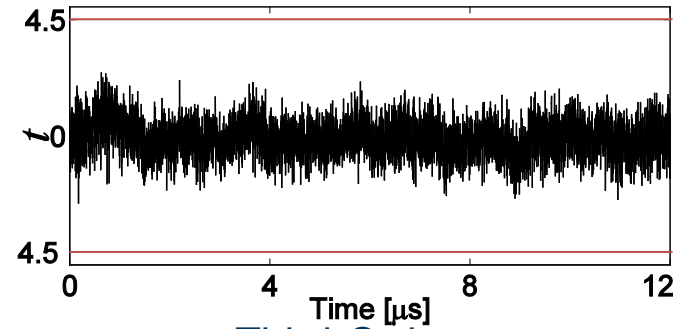
Third-Order

# Evaluation

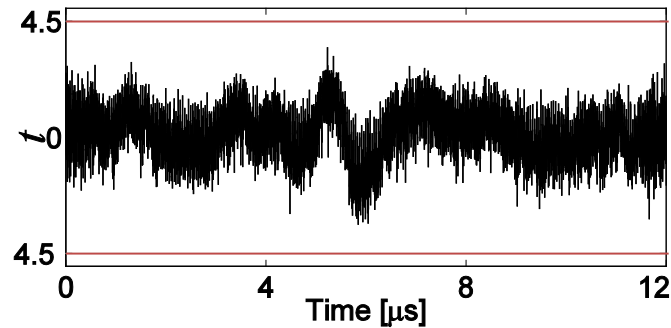
## KATAN-2<sup>ND</sup> (100 MILLION TRACES)



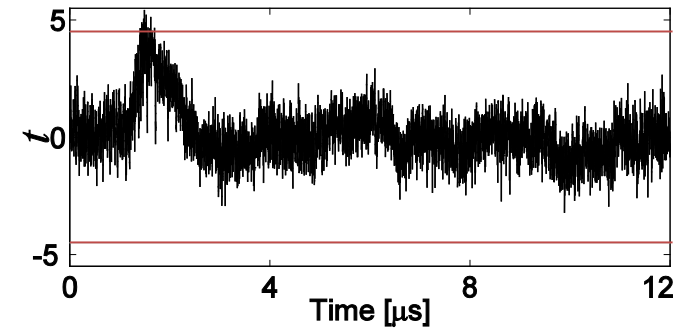
Sample Trace



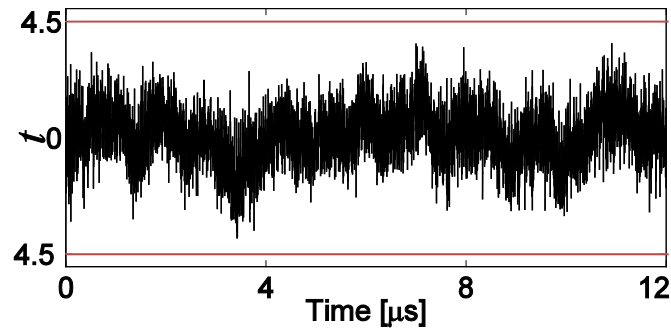
Third-Order



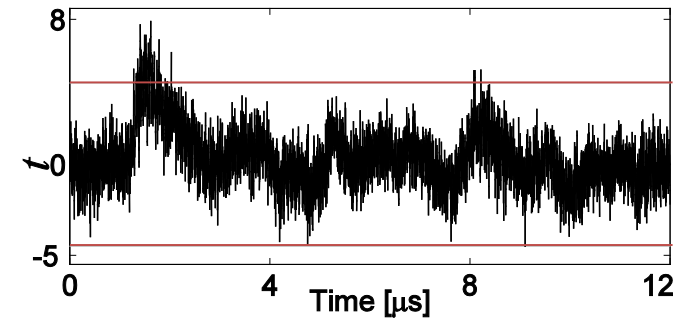
First-Order



Fourth-Order



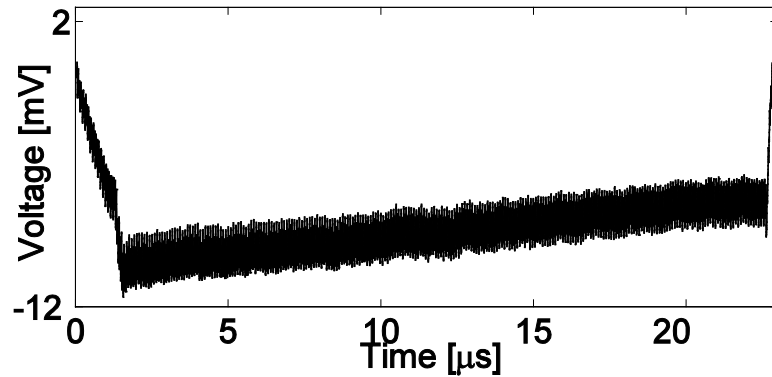
Second-Order



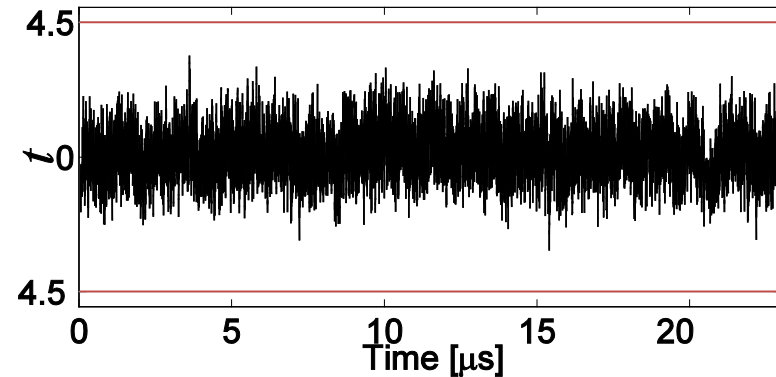
Fifth-Order

# Evaluation

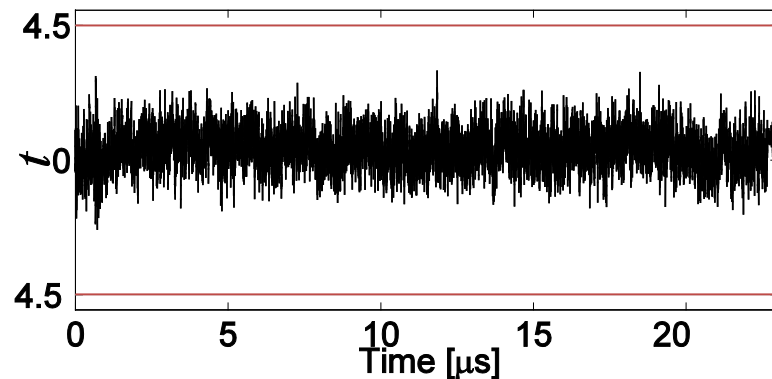
## KATAN-1<sup>ST</sup>-G (1 BILLION TRACES)



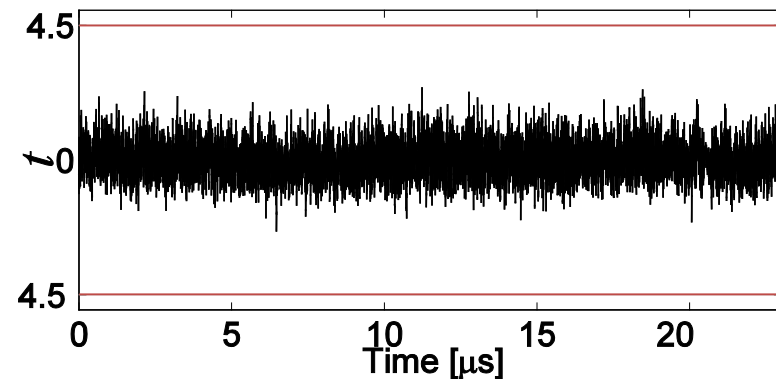
Sample Trace



Second-Order



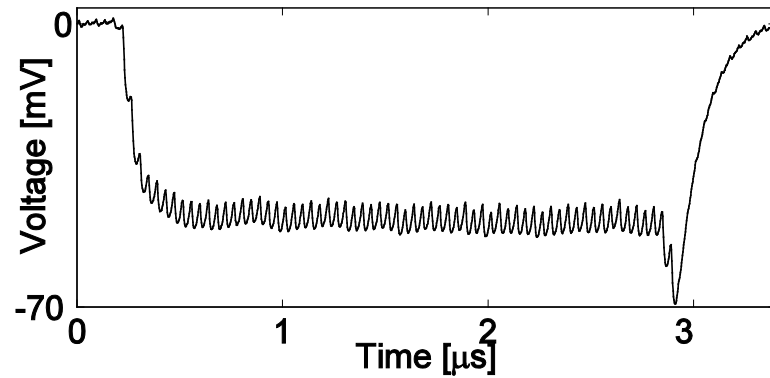
First-Order



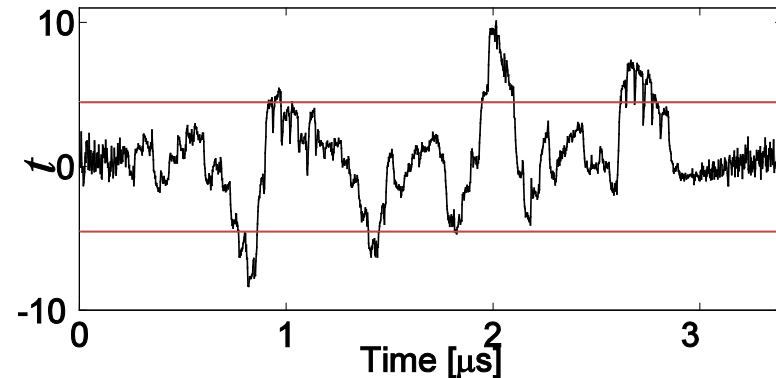
Third-Order

# Evaluation

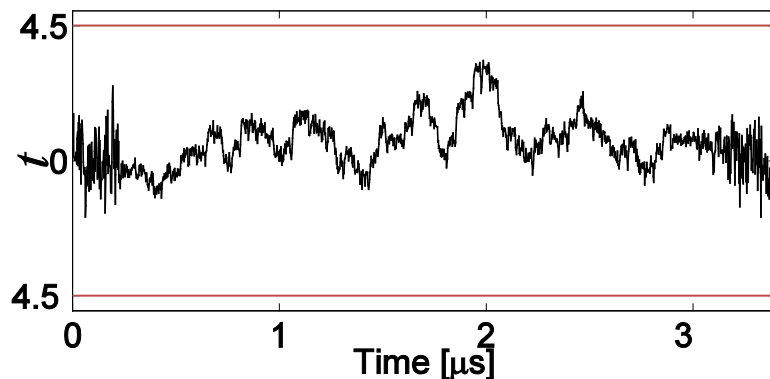
## PRESENT-1<sup>ST</sup> (10 MILLION TRACES)



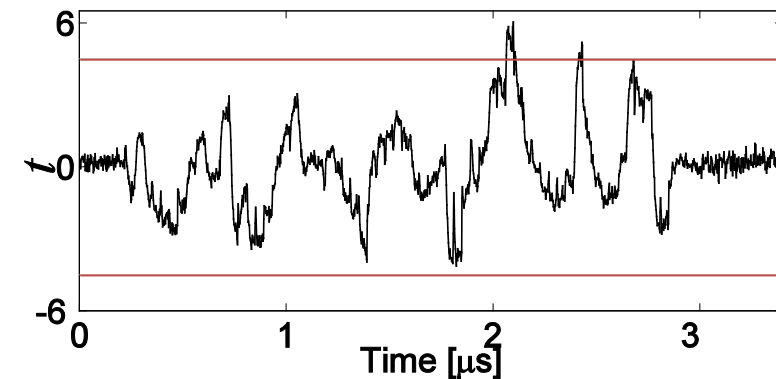
Sample Trace



Second-Order



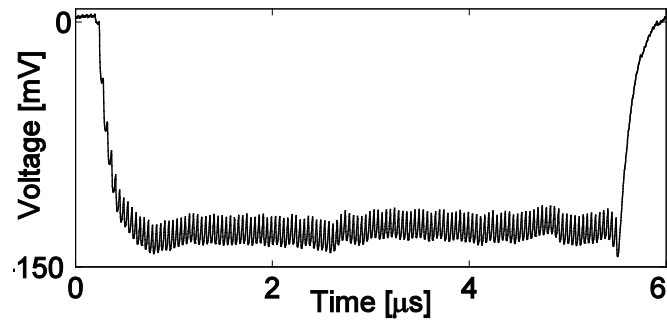
First-Order



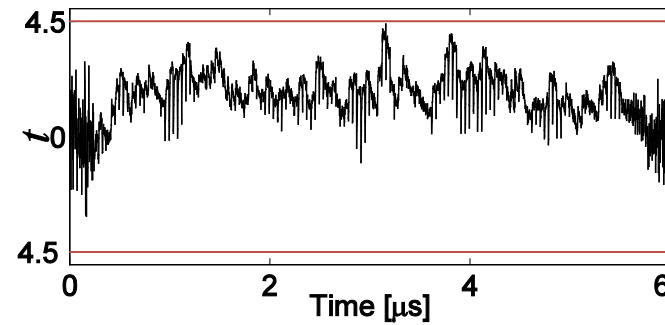
Third-Order

# Evaluation

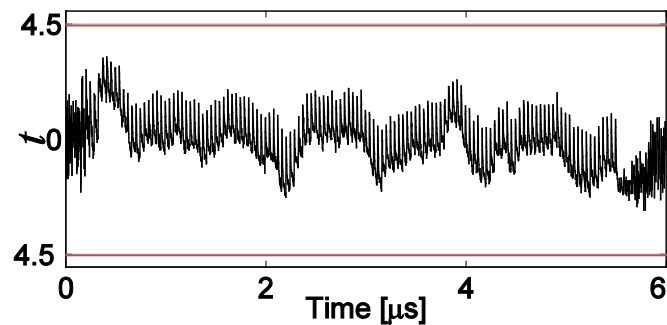
## PRESENT-2<sup>ND</sup> (300 MILLION TRACES)



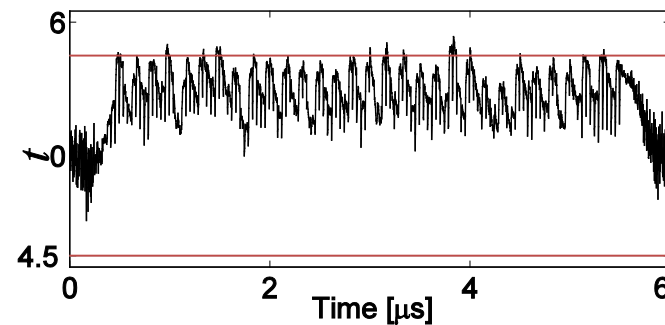
Sample Trace



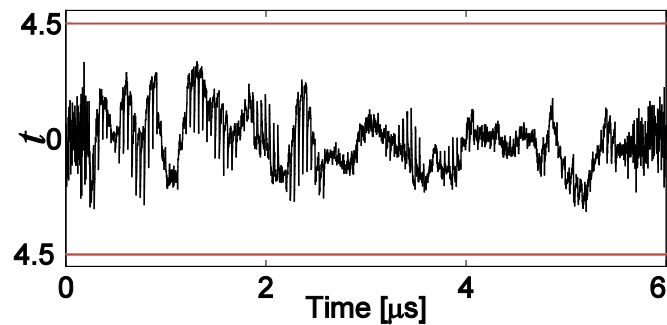
Third-Order



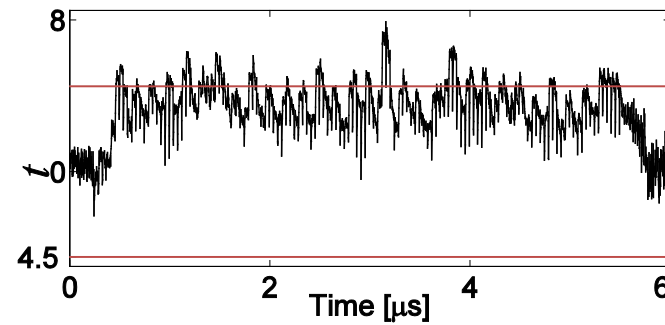
First-Order



Fourth-Order



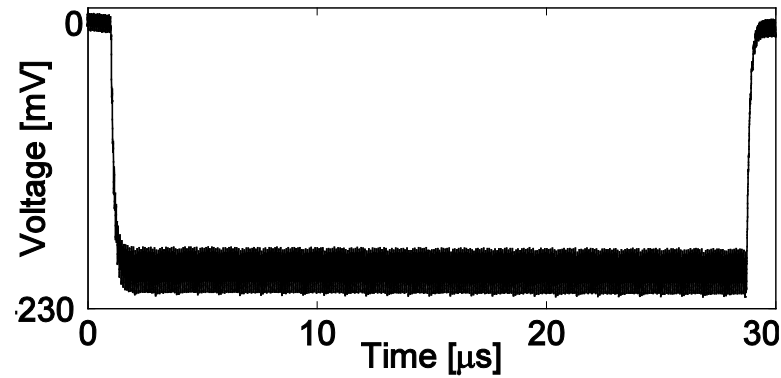
Second-Order



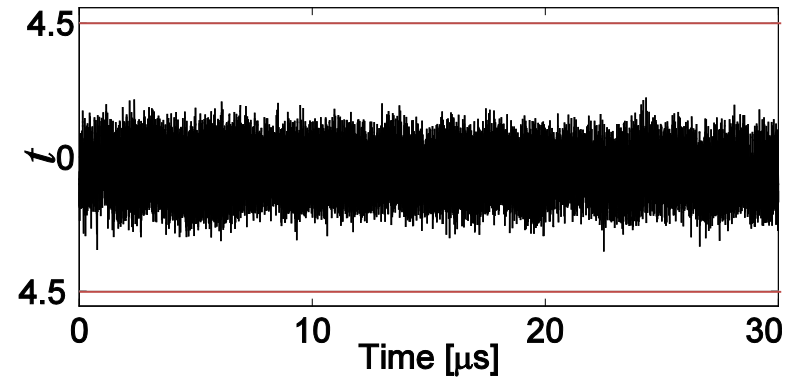
Fifth-Order

# Evaluation

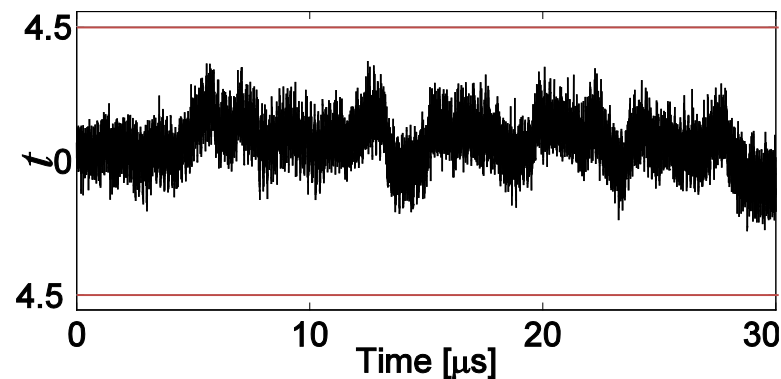
## PRESENT-1<sup>ST</sup>-G (1 BILLION TRACES)



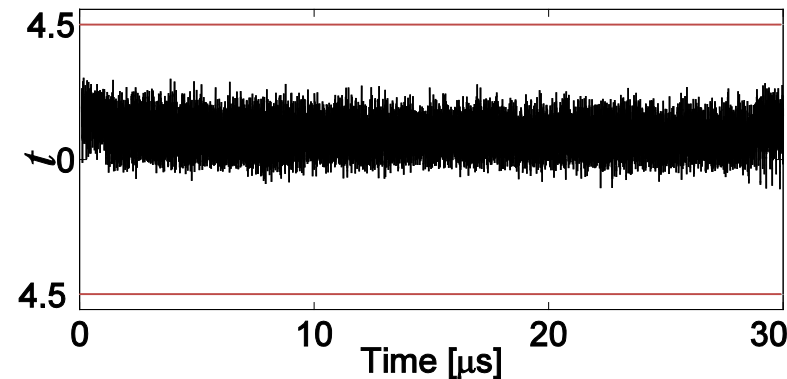
Sample Trace



Second-Order



First-Order



Third-Order

# Conclusion



## Conclusion

GliFreD + TI

## Conclusion

### GliFreD + TI

- Consumes more power

## Conclusion

### GlifreD + TI

- Consumes more power
  - Higher resource utilization

## Conclusion

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  - Natural behavior of power equalization

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  - Design and application dependent

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- Increases latency
  - Design and application dependent
  - Increases frequency → comparable throughput
- Restricted to FPGAs



## Conclusion

### GliFreD + TI

- **Consumes more power**
  - Higher resource utilization
  - Natural behavior of power equalization
- **Increases latency**
  - Design and application dependent
  - Increases frequency → comparable throughput
- **Restricted to FPGAs**
  - ASIC: DPL + TI might have similar security level

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  - Natural behavior of power equalization
- Increases latency
  - Design and application dependent
  - Increases frequency → comparable throughput
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  - Still 1<sup>st</sup>-order secure

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  - Higher resource utilization
  - Natural behavior of power equalization
- Increases latency
  - Design and application dependent
  - Increases frequency → comparable throughput
- Restricted to FPGAs
  - ASIC: DPL + TI might have similar security level
- No provable resistance for higher-order
  - Still 1<sup>st</sup>-order secure
- Higher-order attacks practically infeasible

## Conclusion

### GliFreD + TI

- **Consumes more power**
  - Higher resource utilization
  - Natural behavior of power equalization
- **Increases latency**
  - Design and application dependent
  - Increases frequency → comparable throughput
- **Restricted to FPGAs**
  - ASIC: DPL + TI might have similar security level
- **No provable resistance for higher-order**
  - Still 1<sup>st</sup>-order secure
- **Higher-order attacks practically infeasible**
  - EM analysis

## Conclusion

### GliFreD + TI

- Consumes more power
  - Higher resource utilization
  - Natural behavior of power equalization
- Increases latency
  - Design and application dependent
  - Increases frequency → comparable throughput
- Restricted to FPGAs
  - ASIC: DPL + TI might have similar security level
- No provable resistance for higher-order
  - Still 1<sup>st</sup>-order secure
- Higher-order attacks practically infeasible
  - EM analysis
  - Fair to compare with 3<sup>rd</sup>-order TI

**Thanks for Listening!**

*Any Questions?*